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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,099	01/14/2002	Hiroshi Moriya	500.41080X00	6738

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,099	MORIYA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12 and 17-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *12 and 17-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted claiming priority from U.S. Serial No. 10/043,099 filed January 22, 2002 which itself claims priority under 35 U.S.C. 119(a)-(d), from Japanese Patent Application No. 2001-41097 filed on February 19, 2001 and 2001-8306 filed on January 16, 2001which papers have been placed of record in the file.

Continued Prosecution Application

The request filed on 08/06/2004 for a Request for Continued Prosecution Examination (RCE) under 37 CFR 1.114 (d) based on parent Application No. 10/043,099 is acceptable and a RCE has been established. An action on the RCE follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled on April 01, 2004.

The references on PTO 1499 submitted on 04/01/04 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 08 /06 /2004. Therefore claims 12, 17,18,20,22 and24 as presently amended and claims 19,21 and 23 as previously recited and claims 25 to 37 presently newly added are currently pending in the Application. .

Claim Rejections - 35 USC § 112

Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 25 the phrase "means for decreasing inter atomic distances in the material to suppress leakage current from flowing through the gate insulator" renders the claim indefinite because the term " means "denotes an element in a device whereas the specification as originally only states the decrease in inter atomic distance occurs due a method step that involves the process condition like temperature which step generates the decrease in inter atomic distance.

Claims 26-37 are rejected at least for directly/indirectly depending upon the rejected claim 25.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17,21 and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Matsushita , (Japanese Patent Publication No. 53010283, herein after Matsushita) in view of Okada et al. (U.S. Patent No.5582640, herein after Okada)

With respect to claims 17, 21 and 24, Matsushita describes a semiconductor device including a semiconductor substrate (Abstract line 1 all MOS transistors have a semiconductor substrate), gate insulators formed on said substrate and gate electrodes formed on said insulators (Basic abstract), wherein said gate insulators are composed of a material as a main component selected from titanium oxide, zirconium oxide and hafnium oxide (Basic abstract lines 3-5) and in which compression strain is produced (Basic abstract line 9-10) , said semiconductor device equipped with MOS transistors. (Abstract line 1).

The presently newly added limitation, " So that inter atomic distances in the material are decreased to suppress leakage current from flowing through the gate insulators " cannot be given patentable weight because it is an inherent functional property.

Assuming the newly added limitation is presented in proper format

Matsushita does not specifically describe the newly added limitation so that inter atomic distances are decreased to suppress leakage current from flowing through the gate insulators is an inherent functional property..

However Okada in col. 2 lines 61 to 67 and col. 34 line 64 to col. 35 line 5 , etc. describes so that inter atomic distances are decreased to thereby control the shape and quality of the recrystallized film to provide thin-film transistors and semiconductors integrated circuits having uniform characteristics and high reliability (Okada col. 2 lines 58-66).

Therefore it would have been obvious to one of ordinary skill in the art at the time o f the invention to include Okada's step of decreasing the inter atomic distances in Matsushita's device to thereby control the shape and quality of the recrystallized film to provide thin-film transistors and semiconductors integrated circuits having uniform characteristics and high reliability (Okada col. 2 lines 58-66).

The limitation "to suppress leakage current from flowing through the gate insulators" is a taken to be an inherent functional property for which patentable weight cannot be given.

As stated by the courts in ex parte Masham, " It has been held that a recitation with respect to the manner in which a claimed apparatus (device) in intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham , 2 USPQ 2d 1647 (1987).

As shown above all the structural limitations are obvious in view of the applied Matsushita and Okada references therefore the intended use limitation does not differentiate from the applied references.

With respect to claim 21 Matsushita describes the insulator comprises a film mainly composed of silicon oxide and an overlying film mainly composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide (Matsushita page 438 line 7 from the bottom left hand side column.

With respect to claim 25, to the extent understood, Matsushita describes a semiconductor device including MOS transistors comprising a semiconductor substrate (Abstract line 1 all MOS transistors have a semiconductor substrate), gate insulators formed on said substrate (Basic abstract), gate electrodes formed on said agate insulators (Basic abstract), wherein said gate insulators are comprised of a material as a main component selected from titanium oixde, zirconium oxide and hafnium oxide ((Basic abstract lines 3-5) and means for decreasing interatomic distances in the material to suppress leakage current from flowing through the gate insulator. (Okada in col. 2 lines 61 to 67 and col. 34 line 64 to col. 35 line 5 , etc).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 12-15, 18-20, 22-23 and 26-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita and Okada as applied to claims 17,22, and 24 above and further in view of Van Dover (U.S. Patent No. 6093944 herein after Van Dover).

With respect to claims 18, 20 Matsushita describes a semiconductor device including a semiconductor substrate, gate insulators formed on the substrate and gate electrodes formed on the gate insulators as stated above.

Matsushita does not specifically describe or teach the gate insulator layer is mainly composed of titanium oxide having a retile crystal structure.

However, Van Dover a patent from the same field of endeavor, describes in fig.2 and col. 1 lines 53-56 describes Titanium oxide as gate oxides and col. 6 lines 27-29 for retile) to form (TiO2) dielectric films having sufficiently low leakage currents for reliable use in DRAM devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Andover's titanium oxide in Matsushita's device to form (TiO2) dielectric films having sufficiently low leakage currents for reliable use in DRAM devices.

In which compression strain is produced, and said semiconductor device equipped with Mos transistors (see above under claim 1 above, (Basic abstract line 9-10 Abstract line 1).

Claim 20 further specifies that tensile strain is produced in the gate insulator and tensile strain is produced in the gate electrode (Matsushita describes all types of strain including both the compression and tensile strains being produced in both the gate insulators and the gate electrode)

With respect to claim 19, it repeats all the steps of claim 18 and further adds wherein the thermal expansion coefficient of the main composing material of the gate electrodes is greater than the liner coefficient of the titanium oxide.

Matsushita and VanDover describes all the steps of that are repeated from claim 2 as shown above.

Further VanDover describes a ploy silicon gate in col. 4 lines 40-45 similar to that described in Applicants' specification page 14 lines 3-8 in the same context and for the same purpose and therefore what is true for applicants' (their polysilicon gate wherein the thermal expansion coefficient of the main composing material of the gate electrodes is greater than the liner coefficient of the titanium oxide) is also true for VanDover's polysilicon gate.

With respect to claim 22, it repeats all the steps of claim 18 and further adds that a second MOS transistor has a gate insulator containing silicon oxide in a high proportion. (Matsushita page 438, Van Dover fig.1)

With respect to claim 23, it repeats all the steps of claim 18 and further adds that the first MOS transistor is used for calculations or memories and the second MOS is used for I/O. (Van Dover – Dram or memory device having a memory circuit (calculations or memories) and a peripheral circuit (Imput/Output i.e. I/O).

With respect to claim 24, it repeats all the steps of claim 17 and further adds that the gate insulator has a multiplayer structure (Van Dover fig. 1).

With respect to claim 12, it repeats all the steps of claim 18 and further adds that the main crystal structure of the titanium oxide is anatase (Van Dover col.6 line 29) and the state of strain of the channel region of said semiconductor substrate is tensile strain. (Matsushita Abstract 4th line from last).

With respect to claim 13, wherein a silicon oxide film or a titanium silicate film is deposited between the semiconductor substrate and said titanium oxide gate insulator (Van Dover col. 4 lines 45-50).

With respect to claim 14, wherein the gate electrodes have a phosphorus or boron-added polycrystalline silicon film, (Van Dover claim 7) and a silicon oxide film or a titanium silicate film is inter posed between the gate electrodes and the titanium oxide gate insulators. (Van Dover col. 4 lines 45-50).

With respect to claim 15, wherein the gate electrodes include a tungsten film, a molybdenum film, a tungsten nitride film, a tungsten boride film, a tungsten silicide film or a laminate thereof (Van Dover Van Dover col. 4 lines 50-55).

With respect to claim 26 Mtsushita describes a semiconductor device according to claim 25, wherein said means decreases inter atomic distances between the titanium, zirconium or hafnium atoms and the oxygen atoms in the oxide. (Okada col.2 llines 61-65 insulating films and Matsushita titanium oxide etc. and Okada –reducing distance between Ti, Zr or Hf and oxygen).

With respect to claims 27 and 28 Mtasushita describes a semiconductor device according to claim 25, wherein said means decreases said interatomic distances by producing a compression strain in said gate insulators.(Basic abstract line 9-10)

With respect to claims 29-32 Matsushita describes a semiconductor device according to claim 25, wherein said gate insulators are comprised of titanium oxide as the main component having a rutile crystal structure. (Matsushita page2) .

With respect to claim 33-37 Matsushita describes a semiconductor device according to claim 25, further comprising means for producing a tensile stream in said gate electrode. (Basic abstract line 9-10).

B. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita and Okada as applied to claims 1,5,9 and 11 above and further in view of Van Dover (U.S. Patent No. 6093944 herein after Van Dover). And Lau (U.S. Patent No. 6,249 0898, herein after Lau).

With respect to claim 16, wherein the gate electrodes include a ruthenium oxide film, which is in contact with the titanium oxide gate insulator.

Matsushita and VanDoren do not specifically describe a gate electrode to include ruthenium oxide.

However, Lau, a patent from the same field of endeavor describes in col. 5 line 8

Describes a gate electrode of ruthenium oxide to repair the pinholes in the oxide insulator layers which lead current leakage in the device.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lau's gate electrode of ruthenium oxide in Matsushita and VanDover's device to repair the pinholes in the oxide insulator layers which lead current leakage in the device.

Response to Arguments

Applicant's arguments filed 09/25/2003 have been fully considered but they are moot in view of the new rejection.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

August 18, 2004.

Tuan Quach
Primary Examiner